

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A method of ~~synch~~ynchronising ~~ynchronizing~~ the phase of a local image ~~synch~~ronisation ~~ynchronization~~ signal generator of a local video data processor in communication with an asynchronous switched packet network to the phase of a reference image ~~synch~~ronisation ~~ynchronization~~ signal generator of a reference video data processor also coupled to said network, said local and reference processors having respective clocks, said reference and local image ~~synch~~ronisation ~~ynchronization~~ signal generators generating periodic image ~~synch~~ronisation ~~ynchronization~~ signals in synchronism with said reference and local clocks respectively, said method comprising the steps of:

[[(i)]] frequency ~~synch~~ynchronising ~~ynchronizing~~ said local and reference clocks;

[[(ii)]] said reference video data processor sending, via said network, to said local data processor an image timing packet providing reference image ~~synch~~ronisation ~~ynchronization~~ data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of a reference image ~~synch~~ronisation ~~ynchronization~~ signal; and

[[(iii)]] said local video data processor controlling the timing of production of said local image ~~synch~~ronisation ~~ynchronization~~ signals in dependence on said reference image ~~synch~~ronisation ~~ynchronization~~ data and a time of arrival of said image timing packet.

Claim 2 (Currently Amended): A method according to claim 1, in which said controlling ~~step comprises~~ includes adjusting said time of production of said local image ~~synch~~ronisation ~~ynchronization~~ signal by a correction amount derived from a difference between [[:]] [[(i)]] said reference image ~~synch~~ronisation ~~ynchronization~~ data [[:]] and [[(ii)]]

a time, measured with respect to said local processor's clock and said local image ~~synchronisation~~ synchronization signal, of arrival of said timing packet.

Claim 3 (Currently Amended): A method according to claim 2, further comprising ~~the steps of~~:

[[(i)]] ~~said reference processor~~ sending to said local processor a plurality of said timing packets from said reference processor; and

[[(ii)]] ~~said local processor~~ controlling, by said local processor, said timing of said production of said local image ~~synchronisation~~ synchronization signal in dependence on a function of said differences between:

[[(iii)]] reference image ~~synchronisation~~ synchronization data in said timing packets; and

respective times of arrival of said timing packets at said local processor.

Claim 4 (Original): A method according to claim 3, in which said function is an average of said differences.

Claim 5 (Currently Amended): A method according to claim 1, further comprising: ~~the step of~~ adding a delay to said local image ~~synchronisation~~ synchronization signal.

Claim 6 (Original): A method according to claim 5, in which said delay is a predetermined delay.

Claim 7 (Currently Amended): A method according to claim 1, ~~in which said reference data processor comprises a source of video data produced synchronously with said reference processor's clock,~~ said method further comprising:

[[(i)]] ~~said reference processor~~ sending to said local data processor from said reference processor, via said network, data packets containing said video data, said image timing packets being sent independently of said data packets,

wherein said reference data processor includes a source of video data produced synchronously with said reference processor's clock.

Claim 8 (Currently Amended): A method according to claim 1, ~~in which said reference data processor comprises a source of video data produced synchronously with said reference processor's clock,~~ said method further comprising:

[[(i)]] ~~said reference processor~~ sending to said local data processor from said reference processor, via said network, image timing packets containing said video data and also providing said reference image ~~synchronisation~~ synchronization data,

wherein said reference data processor includes a source of video data produced synchronously with said reference processor's clock.

Claim 9 (Currently Amended): A method according to claim 1, further comprising ~~the step of~~:

[[(i)]] ~~said reference processor~~ sensing, by said reference processor, when said network has capacity to carry an image timing packet; and

[[(ii)]] ~~said reference processor~~ sending, from said reference processor, an image timing packet when such network capacity exists.

Claim 10 (Currently Amended): A method according to claim 1, in which said ~~step~~ of frequency ~~synchronising~~ synchronizing said local and reference clocks ~~comprises~~ includes the steps of:

[[~~(i)~~]] ~~said reference processor~~ sending to said local data processor from said reference processor, via said network, clock timing packets each providing a destination address of said local processor and reference clock data indicating a time at which said clock timing packet is sent; and

[[~~(ii)~~]] ~~said local processor~~ controlling, by said local processor, said frequency of said local processor's clock in dependence on said reference clock data and times of arrival of said clock timing packets.

Claim 11 (Currently Amended): A method according to claim 10, further comprising ~~the steps of~~:

[[~~(i)~~]] ~~said reference processor~~ counting cycles of said reference processor's clock by said reference processor; and

[[~~(ii)~~]] ~~said reference processor~~ setting, by said reference processor, said reference clock data as said count of cycles of said reference processor's clock in dependence on a time at which said clock timing packet containing said reference clock data is launched onto said network.

Claim 12 (Currently Amended): A method according to claim 11, further comprising ~~the steps of~~:

[[~~(i)~~]] ~~said local processor~~ counting cycles of said local processor's clock by said local processor;

[[(ii)]] ~~said local processor~~ generating, by said local processor, local clock data as a count of cycles of said local processor's clock at a time of receipt of a clock timing packet containing reference clock data; and

[[(iii)]] ~~said local processor~~ controlling, by said local processor, said local processor's clock in dependence on an error signal dependent on a difference between said reference clock data in successively received timing packets and a difference between local clock data indicating said local clock time at said times of receipt of said timing packets.

Claim 13 (Currently Amended): A method according to claim 12, further comprising: ~~the step of~~

low pass filtering said error signal to generate a low-pass filtered error signal.

Claim 14 (Currently Amended): A method according to claim 13, further comprising ~~the steps of~~:

[[(i)]] ~~said local processor accumulating~~ receiving said low-pass filtered error signal in said local processor; and

[[(ii)]] ~~said local processor~~ controlling, by said local processor, said local processor's clock in dependence on said received ~~accumulated~~ error signal.

Claim 15 (Currently Amended): A method according to claim 10, in which said clock timing packet containing said reference image ~~synchronisation~~ synchronization data is independent of said reference clock timing packet data.

Claim 16 (Currently Amended): A method according to claim 10, in which said timing packet containing said reference image ~~synchro~~nisation synchronization data also contains said reference clock data.

Claim 17 (Currently Amended): A method according to claim 1, further comprising the step of:

~~said local processor~~ aligning, in said local processor, an image of a video signal with said local image ~~synchro~~nisation synchronization signal.

Claim 18 (Currently Amended): A method according to claim 1, in which said image ~~synchro~~nisation synchronization signal is a field or frame ~~synchro~~nisation synchronization signal.

Claim 19 (Currently Amended): A method according to claim 1, in which said reference image ~~synchro~~nisation synchronization data indicates a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of an immediately preceding reference image ~~synchro~~nisation synchronization signal.

Claim 20 (Currently Amended): A method according to claim 1, in which timing packets carrying information relating to at least two image ~~synchro~~nisation synchronization signals are launched onto said network.

Claim 21 (Currently Amended): ~~Computer software comprising~~ A computer readable storage medium encoded with program code for carrying out a which when executed by a computer cause a processor to carry out the method according to claim 1.

Claims 22-24 (Canceled).

Claim 25 (Currently Amended): A video network, comprising:

[[(i)]] a reference video data processor ~~having~~ including a reference image ~~synchronisation~~ synchronization signal generator and a reference clock generator, said reference ~~synchronisation~~ synchronization signal generator configured to generate ~~generating~~ periodic image ~~synchronisation~~ synchronization signals in synchronism with said reference clock;

[[(ii)]] a local video data processor ~~having~~ including a local image ~~synchronisation~~ synchronization signal generator and a local clock generator frequency-locked to said reference clock generator, said local ~~synchronisation~~ synchronization signal generator ~~generating~~ configured to generate periodic image ~~synchronisation~~ synchronization signals in synchronism with said local clock;

[[(iii)]] an asynchronous packet-based network linking said local processor and said reference processor;

[[(iv)]] said reference video data processor includes a sending unit configured to send ~~comprising means for sending~~, via said network, to said local data processor an image timing packet providing reference image ~~synchronisation~~ synchronization data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of a reference image ~~synchronisation~~ synchronization signal; and

[[v)]]said local processor ~~comprising means for~~ including a controlling unit configured to control timing of production of said local image ~~synehronisation~~ synchronization signal in dependence on said reference image ~~synehronisation~~ synchronization data and said time of arrival of said timing packet.

Claim 26 (Currently Amended): A local video data processor ~~having~~ including a local image ~~synehronisation~~ synchronization signal generator and a local clock generator frequency-lockable to a reference clock generator at a reference video data processor ~~connectable~~ and configured to connect to said local video data processor via an asynchronous packet-based network, said local ~~synehronisation~~ synchronization signal generator configured to generate ~~generating~~ periodic image ~~synehronisation~~ synchronization signals in synchronism with said local clock, [[:]] [(i)]said local video data processor comprising:

~~means for controlling~~ a controlling unit configured to control timing of production of said local image ~~synehronisation~~ synchronization signal in dependence on a received image timing packet providing reference image ~~synehronisation~~ synchronization data received indicating a difference in timing, measured with respect to a clock of said reference processor, between a time at which the image timing packet is launched onto said network and a time of production of a reference image synchronization signal, provided by [[a]] the image timing packet from said reference clock generator and a time of arrival of such a the image timing packet.

Claim 27 (Currently Amended): A reference video data processor, comprising:
having
a reference image ~~synehronisation~~ synchronization signal generator and a reference clock generator;[[,]]

said reference ~~synchro~~nisation synchronization signal generator configured to generate ~~generating~~ periodic image ~~synchro~~nisation synchronization signals in synchronism with said reference clock;

said reference processor ~~being connectable~~ configured to connect via an asynchronous packet-based network to a local video data processor having a local image ~~synchro~~nisation synchronization signal generator and a local clock generator frequency-lockable to said reference clock generator, said local ~~synchro~~nisation synchronization signal generator configured to generate ~~generating~~ periodic image ~~synchro~~nisation synchronization signals in synchronism with said local clock;

[[(i)]] said reference video data processor ~~comprising~~ including a phase synchronization unit configured to synchronize a phase of the local image synchronization signal generator and a phase of the reference synchronization generator by means for sending, via said network, to said local data processor an image timing packet providing reference image ~~synchro~~nisation synchronization data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of a reference image ~~synchro~~nisation synchronization signal.

Claim 28 (Previously Presented): An asynchronous switched network comprising a plurality of nodes, at least one of which nodes is coupled to a data processor that carries out the method of claim 1.

Claim 29 (Currently Amended): A computer readable storage medium encoded with a reference timing packet for use in an asynchronous switched packet network in which packets of video data are transmitted from a source to a destination, said packet providing a

destination address of a processor and reference image ~~synch~~ronisation synchronization data indicating a difference in timing, measured with respect to a reference clock, between a time at which said packet is launched onto said network and a time of production a reference image ~~synch~~ronisation synchronization signal.